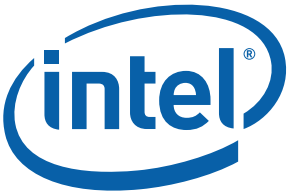


Intel® 6300ESB I/O Controller Hub (ICH)

Specification Update

October 2007

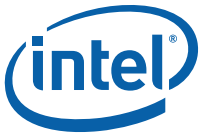
Notice: The Intel® 6300ESB I/O Controller Hub may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Order Number: 300884-012

Contents

Revision History

Date	Version	Description
February 2004	001	Initial release.
March 2004	002	Added Documentation Change 2, SMBus clock operating frequency.
June 2004	003	Documentation Changes: Clarified WDT Reload register bit details; listed USB HS reference voltage register bits.
September 2004	004	Updates to Errata and Documentation Changes.
December 2004	005	Updates to Errata: Configuration Register default. All previous changes and clarifications have been included in the latest revision of the Datasheet (300641-003).
January 2005	006	Added Specification Change: Vcc Power Sequencing Added Specification Clarifications: Vcc Supplies clarification, ACPI C2 state, APIC interrupt, APIC three wire bus references Update to Document Changes: APIC1 Alternate Base Address Register
August 2005	007	Added Errata: Infinite Retries Due To Discard Timer Issue Added Specification Clarification: LPC Cycle Clarification Added Documentation Change: Case Temperature Range
November 2005	008	Added Specification Clarification: 3.3V/1.5V Power Rail Sequencing Added Specification Clarification: Processor Speed Strapping References
March 2006	009	Added Errata: SATA Transport Layer, Alternate Status Added Specification Clarification: GPIO_USE_SEL2 clarification Added Documentation Change: PCIRST clarification, GPO_BLINK default value, Power Plane Usage Model Figure, Advanced Interrupt Controller, GPIO[21] after reset
May 2006	010	Added Specification Clarification: 16550 Compatible Serial Ports, Baud Rate Examples table, Processor Interface Power Management, ACPI C2 state support
February 2007	011	Added Errata: Read of UART IIR Register returns incorrect data, PCI devices on the PCI-X bus when using GPIO[16] Added Documentation Change: PCI-X Rev 1.0 Specification at 66 MHz, V5REF Reference Signal, APIC Indirect Registers, APIC Redirection Table, Power Management Timings Table
October 2007	012	Removed Specification Change 1 and incorporated into datasheet Removed Specficiation Clarifications 1 - 12 and incorporated into datasheet Removed Documentation Changes 2 - 13 and incorporated into datasheet



Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® 6300ESB I/O Controller Hub (ICH) Datasheet	300641-004

Nomenclature

Errata are design defects or errors. Errata may cause the Intel® 6300ESB ICH behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Summary Table of Changes

The following table indicates the specification changes, errata, specification clarifications, and documentation changes that apply to the Intel® 6300ESB I/O Controller Hub (ICH). Intel may fix some of the errata in a future stepping of the component(s), and will account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

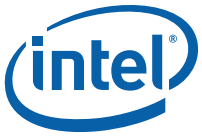
X:	Errata exists in the stepping indicated. Specification change or clarification applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.



Errata

Number	Steppings	Status	ERRATA
	A3		
1	X	No Fix	Board workaround for PCI-X secondary bus reset functionality
2	X	No FIx	Behavior of Serial Port Interrupt Enable Register
3	X	No Fix	USB 2.0 incorrect periodic frame list pointer fetch
4	X	No Fix	Configuration Register default
5	X	No Fix	Infinite retries due to discard timer issue
6	X	No Fix	SATA Transport Layer
7	X	No Fix	Alternate Status
8	X	No Fix	Read of UART IIR Register returns incorrect data
9	X	No Fix	PCI devices on the PCI-X bus when using GPIO[16]

Documentation Changes

Number	DOCUMENTATION CHANGES
1	PCI Device Revision ID

Identification Information

Markings

Stepping	S-Spec / Q-Spec	Top Marking	Notes
A3	Q667	FW80001ESB	Engineering sample
A3	SL76G	FWE6300ESB	Production release

Errata

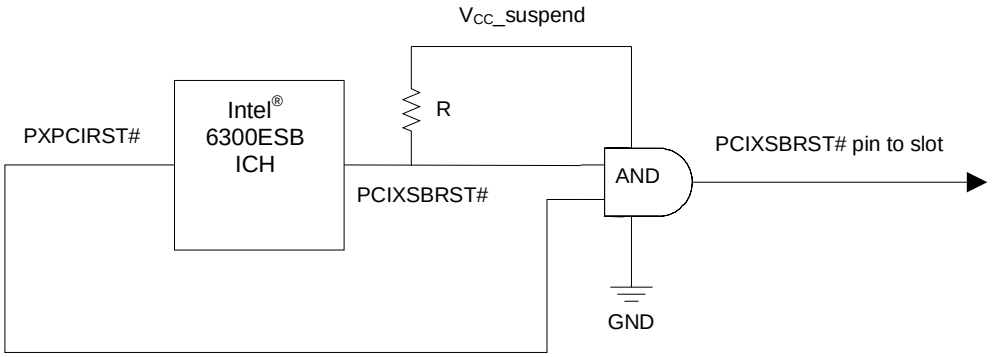
1. Board workaround for PCI-X secondary bus reset functionality

Problem: The Secondary Bus Reset pin (PCIXSBRST#) on the PCI-X bus is internally tied to the Vcc_core well. When the system goes into S3 state (sleep), this signal is floating due to Vcc_core going away.

Implication: System will not WOL when PCIXSBRST# is connected directly to the PCI-X slots.

Workaround: A board workaround pulls the PCIXSBRST# pin up to Vcc_suspend through a resistor (R). This pin is also ANDed with the PXPCIRTST# pin so that if the PCI-X bus resets, the signal that is routed to the slot reflects the reset. Also, since the AND signal is powered by Vcc_suspend, when the system goes into sleep state (S3), this voltage is still present and the correct voltage is applied to the signal that is routed to the slot. See Figure 1 below.

Figure 1. Board Workaround for PCI-X Secondary Bus Reset Functionality



Note: Usage model for SBR functionality (bit 6). Use a pull-up resistor (R) of 100 to 200 kΩ.

Status: No fix. This board workaround is to be used if customers plan to utilize this SBR feature. If not, the PCIXSBRST# pin is to be not connected.

2. Behavior of Serial Port Interrupt Enable Register

Problem: The Serial Port Interrupt Enable Register (IER) bit 1 [3f9h] (Transmit Data request Interrupt Enable) will not change status if the bit has been set previously.

Implication: Will not cause an interrupt if the register bit has been set already. This hinders the serial ports from being fully 100 percent 16550 compatible.

Workaround: Customers may be able to implement a BIOS workaround to clear out the bit IER bit 1 to '0' before programing the bit to '1'.

Status: No fix.

3. USB 2.0 incorrect periodic frame list pointer fetch

Problem: The USB 2.0 controller may fetch an incorrect periodic frame list pointer when the periodic activity is heavily scheduled and there are large latencies on descriptor requests to memory when running HS isochronous or interrupt traffic.

Note: This has only been reproduced in synthetic test environments.

Implication: There may be intermittent audio pops or lost video frames on USB2 HS devices when the system is heavily loaded in synthetic test environments.

Workaround: None.

Status: No fix.

4. Configuration Register default

Problem: The CNF-Intel® 6300ESB ICH Configuration Register (HUB-PCI—D30:F0 Offset 50 - 51h) does not default to the correct state as determined by design.

Implication: Undesired system behavior may occur if left in the default state.

Workaround: The register default must be programmed by the user. See the *Intel® 6300ESB ICH BIOS Specification Update* for the latest recommendation on programming this register.

Status: No fix.

5. Infinite retries due to discard timer issue

Problem: Due to an issue in the Intel® 6300ESB ICH, the discard timer may not trigger, causing infinite retries. This happens when the last retry occurs and within 2 clock cycles later the same data is getting filled into the pre-fetch buffer and the data is never read. The resulting behavior is that the 4K block of memory containing the address is blocked from the agent until the current transaction is completed (However, other agents will be able to access data in this 4K block.)

Implication: Infinite retries may be seen on the PCI-X bus when running in PCI mode, resulting in poor performance and/or undesired system behavior.

Workaround: Options available:

- Ensure that the PCI device used continuously generates a read request until actual data transfer occurs.
- Design a PLD which can monitor continuous retries and trigger an interrupt after “n” number of retries. Interrupt service routine can issue secondary bus reset to come out of continuous retry state for the card of the requested data.

Status: No fix.

6. SATA Transport Layer

Problem: The Intel® 6300ESB ICH does not retry non-data FIS errors. SATA Specification Rev 1.0 implies that non-data FIS errors be retried via hardware.

Implication: None known. Non-data FIS errors will be retried via software (driver).

Workaround: None.

Status: No Fix.

7. Alternate Status

Problem: In native mode IDE, when the Alternate Status Register for SATA device 1 is accessed and there is not a device connected, the register value is decoded as a 50h (device present) instead of 00h (device not present).

Implication: Warning message may occur in some Linux operating systems indicating a discrepancy between the Alt Status and the Status registers. Linux will use the correct Status register data and continue execution.

Workaround: None.

Status: No Fix.

8. Read of UART IIR Register returns incorrect data

Problem: A race condition is observed when reading the IIR register, Transmit FIFO request data bit, at the same time that the UART is updating it, it is possible for the IIR to return incorrect data. This can result in the loss of interrupts. The use of the STPCLK signal exacerbates this condition. The problem was discovered enabling STPCLK with a fixed

duty cycle while the interrupt routine is being service, delays code execution. The execution delay introduced facilitates the race condition, but it's not limited to STPCLK used.

Implication: This condition is seen when using the chipset combination of the 6300ESB ICH & 855GM MCH, Serial port operating at a baud rate of 115200 and when STPCLK throttling is enabled.

Workaround: None.

Status: No Fix.

9. PCI devices on the PCI-X bus when using GPIO[16]

Problem: Unexpected system behavior will occur when the following configuration is used.

- The PCI-X Bus of the Intel® 6300ESB ICH is in PCI mode
- GPIO[16]/PXGNT[2]# is configured as a GPIO (Offset 00h: GPIO_USE_SEL - bit 16 set to a 1)
- GPIO[16] level is toggled continuously (Offset 0Ch: GP_LVL: GPIO Level for Input or Output - bit 16 toggled from a 0 to 1)

Implication: PCI devices on the PCI-X bus hang or demonstrate undesired behaviors when the above configuration is used.

Workaround: When the PCI-X bus of the Intel® 6300ESB ICH is used in PCI mode, it is recommended not to use GPIO[16]. Instead, use any other available GPIO in the system.

Status: No Fix.

Documentation Changes

1. PCI Device Revision ID

Issue: PCI Revision ID Register Values (PCI Offset 08h) for all Intel® 6300ESB ICH functions are shown below.

Table 1. PCI Device Revision ID Table

Intel® 6300ESB ICH Rev IDs					
Device Function	**Descriptions**	**Device ID**	**A0 Rev ID**	**A1/A2 Rev ID**	**A3 Rev ID**
D30:F0	HL-PCI	244E	08h	09h	0Ah
D31:F0	LPC bridge	25A1	00h	01h	02h
D31:F1	IDE	25A2	00h	01h	02h
D31:F2	SATA	25A3	00h	01h	02h
D31:F3	SMBus	25A4	00h	01h	02h
D31:F5	AC97*	25A6	00h	01h	02h
D31:F6	AC97 Modem	25A7	00h	01h	02h
D29:F0	USB1.1 F0	25A9	00h	01h	02h
D29:F1	USB1.1 F1	25AA	00h	01h	02h
D29:F4	WDT	25AB	00h	01h	02h
D29:F5	APIC1	25AC	00h	01h	02h
D29:F7	USBe*(2.0)	25AD	00h	01h	02h
D28:F0	PCI-X	25AE	00h	01h	02h

Affected Docs:Intel® 6300ESB I/O Controller Hub (ICH) Datasheet, Revision 004